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Can We Build a Truly High Performance Computer Which is Flexible and Transparent?

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State-of-the art computers need high performance transistors, which consume ultra-low power resulting in longer battery lifetime. Billions of transistors are integrated neatly using matured silicon fabrication process to maintain the performance per cost advantage. In that context, low-cost mono-crystalline bulk silicon (100) based high performance transistors are considered as the heart of today's computers. One limitation is silicon's rigidity and brittleness. Here we show a generic batch process to convert high performance silicon electronics into flexible and semi-transparent one while retaining its performance, process compatibility, integration density and cost. We demonstrate high-k/metal gate stack based p-type metal oxide semiconductor field effect transistors on 4 inch silicon fabric released from bulk silicon (100) wafers with sub-threshold swing of 80 mV dec^{-1} and on/off ratio of near 10^4 within 10% device uniformity with a minimum bending radius of 5 mm and an average transmittance of ~7% in the visible spectrum.

Our today's information technology centered life is credited to silicon based high performance digital electronics (specifically transistors). Continued scaling of device dimensions and ultra-large-scale-integration of billions of devices in tiny areas has made it possible. However, one competing challenge is to achieve high performance and longer battery lifetime to enable ultra-mobile computation. The rapid expansion of silicon technology is also fueled by semiconductor industry's highly reliable manufacturing process and its cost effectiveness, which starts with the substrate price. Therefore, ultra-mobile computation rapid dissemination will take place when we will have high performance and multi-tasking capable small and ultra-light-weight affordable computation gadgets with ultra-high-capacity memory, bright resolution displays and extra-long battery lifetime. Additional game changer will be flexible and transparent devices for wide deployment of such gadgets. In general, flexible and transparent electronics is a growing market which is expanding rapidly and whose scientific interest has increased exponentially in the recent years. Yet an elusive goal is to achieve truly high performance flexible and transparent computation devices in a cost-effective manner. Different kinds of approaches have been explored but this lofty goal is still to be attained. On one side, low cost and flexible organic materials have already proved their resourcefulness, being the leading option for commercial flexible LED screens[1,2]. However, their fundamentally moderate electrical mobility limits their application in electronics devices capable of competing against today's most advanced silicon-based devices. As an example, recent high performance organic semiconductors report mobilities in the order of 10^{-1} cm^2 V^{-1} s^{-1}, which are only 4% the values for inorganic materials[3,4]. Furthermore, they are not compatible with high-thermal budget processes, usually used during the fabrication of electronics devices. Recently very high mobility in the order of 10^3 cm^2 V^{-1} s^{-1} have been reported with aligned arrays of single-wall carbon nanotubes (SWCNTs) and by using atomic crystal structure graphene[5,6]. Medium-scale integrated circuits have also been demonstrated with more modest, yet competitive values in the order of 10 cm^2 V^{-1} s^{-1} by using SWCNT random networks with solution deposition techniques[7]. Although these results are encouraging, the integration level demanded by the high performance computing in portable devices, which features the most advanced silicon-based transistors with billion devices and nano-sized architecture, is at this stage not feasible with this kind of techniques. Additionally graphene is a low band gap semi-metallic film, which does not show on/off behavior thus its application is more inclined towards radio-frequency (RF) applications. In recent years several efforts have been made to combine the excellent electrical performance of silicon with the mechanical flexibility and support of polymer-based materials[8–12]. Thin film transistors have been fabricated using mono-crystalline silicon nano-ribbons or micro/nano-membranes, also known as micro-structured silicon (μs-Si), usually released from silicon-on-insulator (SOI) or silicon (111) or (110) substrates[13–15]. Polymeric materials such as polymide (PI), polyurethane (PU), polyethylene terephthalate

(PET) or polydimethylsiloxane (PDMS) then serve as flexible mechanical support for the transfer of μs-Si sheets. After the transfer process, transistors are built by different printing technologies and circuitry of different complexity can be achieved[16]. Inarguably and logically these innovations are directed towards energy and bio-integrated electronics. For the rapid expansion of high-performance ultra-mobile computation SOI substrates are expensive options compared to the most common silicon (100). Silicon (111), on the other hand, is not only expensive but also presents higher defect density[17,18], and with silicon (110), even though its wet-chemical-based release method might represent a cheaper approach, the performance achieved, specially for electron transport mobility, is still far from expectations[15]. In spite of the relatively high complexity achievable through this technology, the extremely high resolution needed for nano-metric alignment, a customary task in semiconductor manufacturing, represents a major threshold for this technology to reach the ultra-large-scale-integration (ULSI) density required in today's portable electronic devices industry. Finally high thermal budget processes are routine and well-established practice during fabrication of complementary metal-oxide-semiconductor (CMOS) technologies. For example, it allows threshold voltage tuning and removal of trapped charges in the dielectric. Unfortunately polymeric substrates are intolerant to such temperature treatment. An alternative approach for flexible electronics manufacturing consists on fully fabrication of devices on silicon substrates followed by the use of specific processing methodologies to thin down the substrate's thickness and achieve bendability. Polishing or grinding the backside of the wafer is one of the most common thinning technologies used routinely in today's industry, however grinding to a few tens of micrometers in thickness, needed for good bendability, produces substrate damage and non-uniformity, thus reducing the yield, not to mention the waste of material removed during the process. Recently, a new technique has been developed to produce thin substrates out of standard wafers by exfoliation or *spalling* processing[19,20]. A nickel layer is deposited on top of passivated devices, building up stresses on the substrate which leads to a fracture at a specific depth, mainly determined by amount of stress, so a thin top portion of the wafer can be controllably peeled off. Ultra-thin body silicon on insulator (UTB-SOI) has been used with this technique to achieve very thin thickness and high performance, but it comes with the very high cost of such substrate and process, limited bendability and opaqueness in nature. Another methodology has been explored where initially a porous silicon double layer is formed with two-steps anodic etching allowing the bottom less-denser layer to be removed after a high-thermal budget process. This way, a released porous silicon membrane is created that hangs on top of the substrate. Epitaxial silicon is then grown on top where devices can be fabricated as done on an ordinary wafer. Finally the released areas can be peeled off from the substrate and be transferred onto a plastic carrier substitute substrate[21,22]. Even though integrated circuits of high complexity has been demonstrated with this technique, moderate bendability, opaqueness, limited throughput and less economically attractive procedures, such as ultra-expensive UTSOI substrate, silicon epitaxy and unconventional micro-fabrication processes like anodic etching, detours its compatibility with main-stream silicon foundry. It is to be noted technically it is much easier to have a buffered layered substrate (like in SOI or SIMOX) as it is simpler to etch off that buffer layer to release the top portion as flexible platform but the substrate cost and disposal of that after one time use of the substrate is not an attractive proposition for mainstream semiconductor industries to actively think about using flexible electronics for consumer electronics with huge market potential. The driving force has always been performance per cost both from the manufacturers' and the consumers' perspective. A final alternative is to work directly with commercially available ultra-thin silicon wafers. However, they are almost five times more pricy than standard bulk wafers, have higher defects and extreme fragility makes them really hard to handle and almost impossible to work with in a typical cleanroom environment.

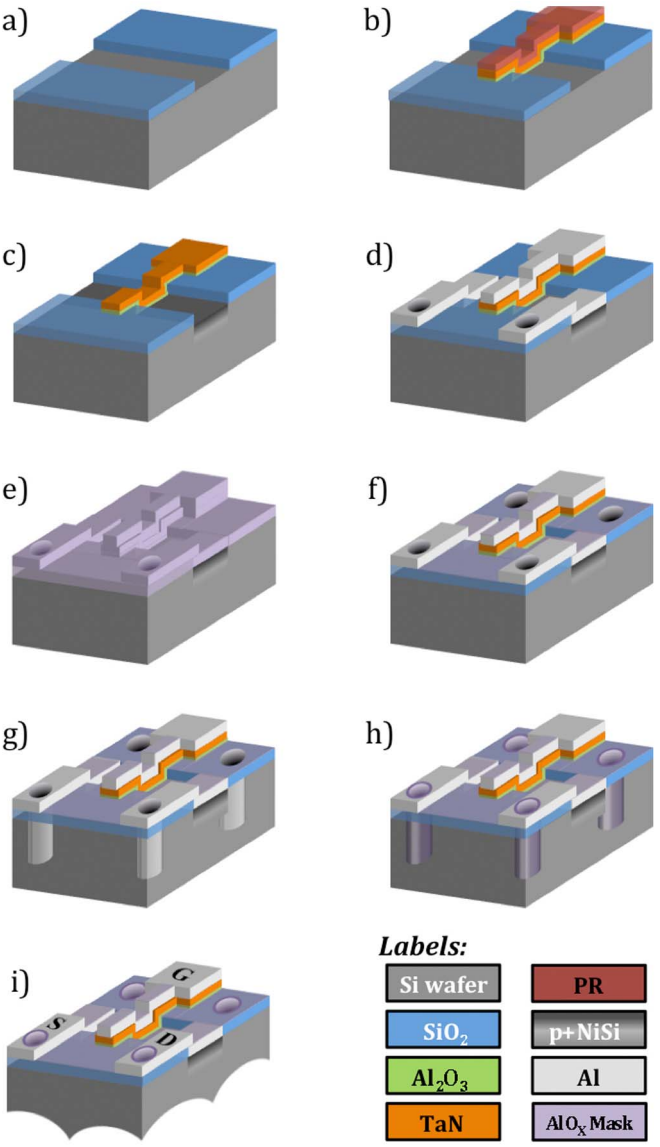

Figure 1 | Fabrication process flow of p-type MOSFET on Si (100) fabric. Detailed description is in the main text.

Results

Fabrication process. The fabrication of p-type MOSFETs relies solely on standard micro-fabrication techniques and it is completely compatible with CMOS processing. Figure 1 depicts the basic steps to fabricate transistors. First, isolation of devices is realized through trench formation on a silicon dioxide (SiO_2) layer denoted from now on as the active area (Fig. 1a). Next high-k/metal gate stack is deposited by atomic layer deposition (ALD) at 300°C. Ultra-thin, uniform and high quality films are conformally deposited. A research-level photolithography process followed by reactive ion etching (RIE) is used to pattern the deposited films with resolution capabilities down to 5 μm (Fig. 1b). Much more complex, industry-level systems could ideally be used for this purpose with the possibility to attain feature sizes of tens of nanometers, thus greatly increasing the performance. The next step consists on the ion implantation (I/I) of dopants to form source and drain regions in the active area. Photoresist (PR) on top of the gate stack acts as

protective layer of the very thin films during the implantation. After PR removal, rapid thermal process (RTP) is used at a very high temperature (950°C for 30 seconds) to electrically activate the dopants, moving impurities from interstitial to substitutional lattice sites, and to recrystallize any amorphization damage resulted after implantation. A fast temperature ramp-up and down is needed to avoid unwanted impurities diffusion. Before metal contact formation and in order to reduce the contact resistance with silicon, we performed a self-aligned silicidation process to form nickel silicide (NiSi) in the source/drain regions, accomplishing thus a very low ohmic contact (Fig. 1c). Nickel is selected over other materials due to its very low sheet resistance when silicided (around 6 $\Omega\,\square^{-1}$) and since it can be formed at relatively low temperatures (450°C). Since long channel devices were fabricated for the present report, nickel diffusion into the channel does not represent a concern and a single-step salicidation process can be used. Nickel is first deposited with sputtering followed by rapid thermal anneal (RTA) to form the silicide only in such areas where the nickel film is in direct contact with silicon, thus denominated as a self-aligned process. The excess nickel is then removed with sulfuric peroxide mixture (SPM). Aluminum sputtering, photolithographic patterning and chlorine-based RIE processing creates the gate and source/drain contacts (Fig. 1d). At this point, holes are formed in the contact pads to aid the future hole-formation over the entire sample area that will be released from the bulk silicon wafer. In order to provide protection of the active area and gate stack from the forthcoming xenon di-fluoride (XeF_2) etching, Al_2O_3 is deposited by ALD on top of all the devices (Fig. 1e). A final photolithographic step is performed to generate etching holes that will be used for the release process. RIE of Al_2O_3 and field oxide (FOX) layers (Fig. 1f) is followed by BOSCH processing, a kind of deep reactive ion etching (DRIE), to create straight channels into the silicon substrate with a depth of around 30 μm (Fig. 1g). Spacer-like sidewall scheme, accomplished through low temperature ALD deposition (250°C) and a very anisotropic RIE process, is used to protect the sidewalls of the silicon channels (Fig. 1h). Further details on spacer-based scheme and the release process in general can be found in our previous works[23–25]. Finally, a thin silicon fabric is released on a xenon di-fluoride (XeF_2)-based etching system by isotropically removing the silicon from the inner portion of the substrate (Fig. 1i). At this point, the thin silicon fabric has been released from the bulk substrate resulting in an extremely flexible platform with semi-transparent property due to etch holes. The remaining bulk substrate after release can be reused after performing chemical-mechanical-planarization (CMP) to flatten the profile left by the isotropic etching property of XeF_2. An additional important final procedure consist on forming gas annealing (FGA) of the released sample at 400°C for 5 minutes. This will help to remove trapped charges in the dielectric, which can directly affect the device's performance. Figure 2 shows scanning electron microscope (SEM) images of representative steps during the fabrication process including the layout of a single transistor (Fig. 2a). The thickness of the sample is 17.5 μm, which is determined by the depth of the trenches done by DRIE minus the amount of silicon isotropically etched upwards during the XeF_2-based release. Additionally, as can be appreciated from the figure, 10 μm holes, separated by 10 μm, are covering the whole layout. The presence of these holes represents in fact an effective area loss of 25.6%, however since the substrate can be reused to fabricate more layers with devices, the loss can be balanced with the possibility of producing up to 5 more thin fabrics from one single substrate[26]. The only design constraint given by the presence of holes is the fact that if we want to avoid having holes through our active area, the maximum allowed channel width is restricted to be less than the distance between holes (10 μm with this design). In the case of ultra-scaled integrated circuits though, transistor's dimensions are way smaller and this would not represent an actual constraint.

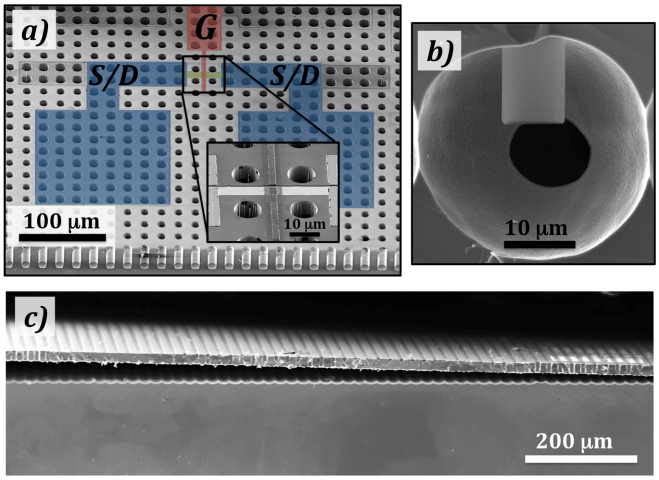

Figure 2 | Scanning electron microscopy images of representative fabrication steps. (a) Transistor layout after DRIE process showing hole distribution and depth. (Inset-Channel area zoomed-in). (b) ALD-based Al_2O_3 spacer after XeF_2 etching showing isotropic profile. (c) Released ~15 μm silicon fabric after completed XeF_2-based release.

Electrical characterization. In order to study the main characteristics of our MOSFETs we measured the I–V characteristics in both the sub-threshold and linear regions. The results are shown in Figure 3 for a representative device. The current at saturation with $V_{GS} = -2$ V is −4.4 μA/μm for $V_{DS} = -2$ V and −0.3 μA/μm for $V_{DS} = -100$ mV. I_{on}/I_{off} ratio is 3.7 decades and the gate leakage is as small as 70 μA/cm² at $V_{GS} = -1$ V.

To start the electrical characterization, we have first determined the threshold voltage by the linear extrapolation method[27], as it is an important parameter required to calculate other parameters such as mobility. Taking the I_D–V_G characteristics at low V_{DS}, ensuring operation in the linear region, the threshold voltage is calculated from,

$$V_{th} = V_{GS\_0} - \frac{V_{DS}}{2} \tag{1}$$

Where, V_{GS_0} is the voltage intercept of the extrapolated linear region in the I_D–V_G curve. From equation (1) and Figure 3b we get a threshold voltage of −0.44 V. Another important parameter in the MOSFET characterization is the mobility, which directly influences the performance of the device. Effective mobility can be extrapolated from the I–V characteristics in the linear region. At low drain voltages, mobility can be estimated from[28],

$$\mu_{eff} = \frac{L}{W}\frac{g_d}{C_{ox}(V_{GS} - V_T)} \tag{2}$$

Where, C_{ox} is the oxide capacitance, W and L are the channel width and length respectively, V_{GS} and V_T are the gate and threshold voltages, respectively and g_d is the drain conductance given by,

$$g_d = \frac{\partial I_D}{\partial V_{DS}} \tag{3}$$

Drain conductance can be extracted from the slope in the drain output characteristics, given by the I_D–V_D curves (Figure 3c), at low V_{DS}. C_{ox} was measured separately and details can be found in the supporting information (SI), Fig. S1. From equation (3) we estimated then the effective mobility to be 43 $cm^2\,V^{-1}\,s^{-1}$. In this case this mobility represents the hole-mobility as we have a p-type MOSFET device.

Finally, sub-threshold swing, also known as inverse sub-threshold slope (S), can be easily extracted from the slope in the I_D–V_G curve with logarithmic scale. From Figure 3a, S = 80 mV dec^{-1}, a neat value to indicate ultra-fast switching.

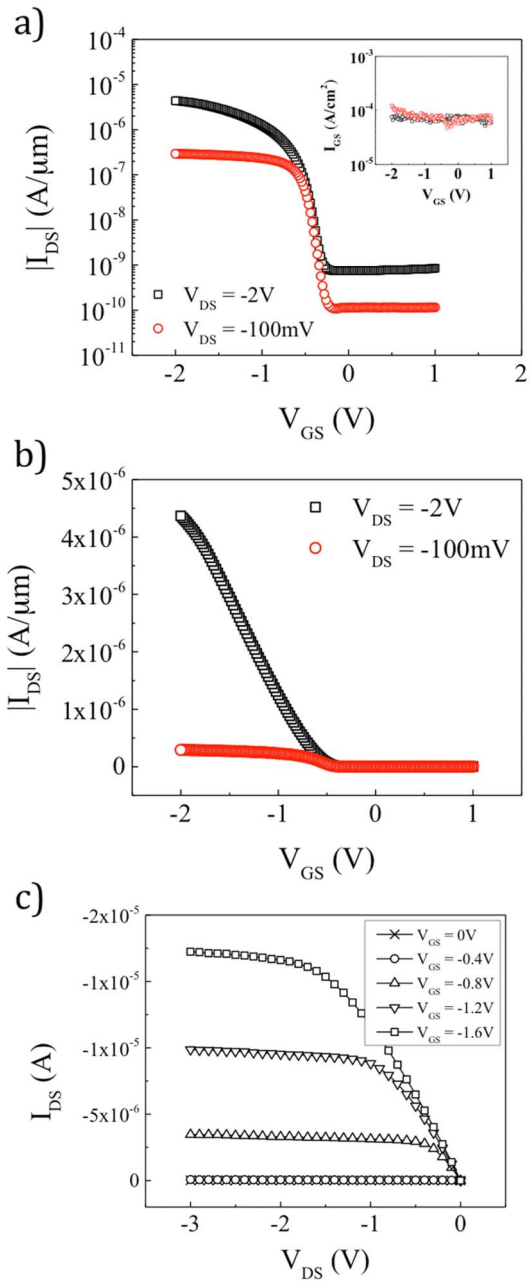

Figure 3 | Electrical performance of a representative device on a released fabric (L = 8 μm, W = 5 μm). (a) I_D–V_G transfer characteristics in logarithmic scale (Inset-Gate leakage density current). (b) I_D–V_G transfer characteristics in linear scale. (c) I_D–V_D curves of same transistor.

All together the results here reported showed competitive values (Table 1), even though there is still a lot of room for improvement. The parameters reflect mainly the capabilities of the research facilities and the available material set. The use of a much more optimized fabrication facility, such as an industrial semiconductor foundry, would certainly result in highly performance devices[19–22]. Some important improvements for future devices are currently being explored. First, the isolation scheme can be drastically improved by implementing shallow trench isolation (STI) in the design. A multiple implantation scheme will not only allow the implementation of complementary logic but will also allow better threshold voltage adjustment, among others. Gate spacers can also be included for protection during implantation and salicidation. Even more relevant, scaling-down of the main features will also highly increase current generation and performance in general.

In order to have a better understanding of the implications associated with the release method and the related sub-processes, we have compared the electrical performance of a sample before and after release processing. Figure 4 compares the I_D–V_G transfer characteristics in the saturation and sub-threshold regime of the same transistor before and after release. As can be observed there is a small current reduction, around 2.6%, in the saturation region of the transistor (Figure 4a). In fact, due to the presence of strained oxide on top the silicon for insulation of devices, there is a small residual strain which can contribute to the reduction in current and other parameters, as will be discussed in the upcoming section. The increase in I_{off} current, up to one decade, from ~30 pA/μm to ~300 pA/μm, can be related to the reduced substrate thickness, which makes the sample more susceptible to noise or thermal excitation allowing more off-state leakage. Gate leakage current for unreleased and released samples is shown in Figure 4c. We observed a small increase in leakage although it does not represent a significant difference. Additionally we have extracted the threshold voltage (V_{th}) and the sub-threshold swing (S) from both released and unreleased samples. The threshold voltage in the released sample showed a reduction around 7%, most likely related to the current reduction, from −0.48 V in the unreleased sample to −0.45 V in the released one. The sub-threshold swing, on the other hand, showed an insignificant change, increasing from 75.24 mV dec^{-1} in the unreleased sample to 80.3 mV dec^{-1} in the released one, representing a 6.7% increase. In summary, besides the off-current, less than 10% variation in main parameters results from the additional processing related to the release method. This can be attributed to the residual strain as a result of the oxide and other deposited layers on the fabric. On the other hand, even though the I_{off} current, and therefore I_{on}/ I_{off} ratio, are significantly affected, the values remain at an acceptable and competitive level.

Mechanical study. Mechanical characterization started with the measurement of the minimum bending radius of the sample (Fig. 5a). Higher bendability is possible thanks to the presence of holes as previously demonstrated with an increase in bendability up to 64% compared with a sample without holes[25]. A bending radius of 5 mm was achieved with 66% applied strain (estimated as dL/L, where L is the initial length of the sample and dL is the horizontal displacement done to achieve such specific radius)[29]. We have also calculated the nominal strain at the top surface of the fabric where the transistors are located. The nominal strain can be obtained from,

$$\varepsilon_{nom} = \frac{t}{2R} \tag{4}$$

Where, t is the thickness of the fabric and R is the bending radius. Details on how to derive equation (4) can be found in the supporting information (SI). As can be appreciated, the strain depends inversely on the radius (Fig. 5b). At 5 mm bending radius, the sample is thus subject to a nominal tensile strain of 0.174% in longitudinal direction with the transistor's channel. As mentioned previously, after the release process the sample was already under a small residual strain. In order to calculate this value we first need to determine the nominal radius at which the sample is bended after release. An approximate method can be used for this purpose, where the bending radius is calculated by[30],

$$R = \frac{L^2}{\pi^2 h_0} \tag{5}$$

Where, h_0 is the deflection of the substrate in the z direction at the center of the sample. Equation (5) gives a value of 69.2 mm for h_0 = 1.3 mm. Now, by using equation (4) we obtained a residual strain of 0.0126% (Fig. 5b). It is also of our interest to know the effect of the bending radius, or nominal strain, in the electrical behavior of the transistors. With this aim, we have measured different important parameters that characterize our devices at different bending radii

Table 1 | Transistor performance comparison between different technologies for flexible electronics development

Reference	This paper	[19]	[22]	[13] [a]	[14] [a]	[15] [a]	[7]	[4]
Technology	Spacers + XeF_2 release	Exfoliation	Epi-Si grown on Porous-Si	Release from SOI + transfer	Release from bulk + transfer	Release from bulk + transfer	Soft-lithography on plastic	Organic semiconductor
Substrate	4" Si (100) n-type (10–20 Ω cm)	8" Si (100) -	4" Si (100) p-type (0.01–0.02 Ω cm)	6" SOI p-type (13.5–22.5 Ω cm)	Si (111) p-type (8–15 Ω cm)	Si(110) p-type (7.5 ± 0.6 Ω cm)	-	-
Channel material	Si (100)	Si (100)	n epi-Si (100)	μs–Si (100)	μs–Si (111)	μs–Si (110)	SWCNT	Tetracene
Dielectric	Al_2O_3 (10 nm)	SiO_2 (20 Å)	- (40 nm)	SANDs (~15 nm)	SiO_2 (50 nm)	SiO_2 (80 nm)	HfO_2 (40 nm)	Air gap (4.9 μm)
Final thickness	17 μm	25 μm	1.5 μm (Si) + - (Plastic)	150 nm (SOI) + 70 μm (PI)	0.8–11 μm (Si) + 1.2 μm (PI)	~5 μm (Si) + 10 μm (PU) + 100 μm (PET)	- (PI)	- (PDMS)
Gate length (L) [μm]	8	0.15	4	7.5	20	30	50–100	100–200
Channel width (W) [μm]	5	10	100	100	80	180	200	330 [b]
W/L Ratio	0.625	66.66	25	13.33	4	6	4–2	3.3
I_{ON} [μA μm^{-1}]	4.4 (-2 V_{DS}, -2 V_{GS})	150 (-1 V_{DS}, -1 V_{GS})	20 (-3 V_{DS}, -5 V_{GS})	1 (50 mV_{DS}, 2 V_{GS})	6.25 (2.1 V_{DS}, 3 V_{GS})	0.12 (0.1 V_{DS}, 10 V_{GS})	0.125 (-5 V_{DS}, -2 V_{GS})	0.0015 (-10 V_{DS}, -50 V_{GS})
I_{OFF} [pA μm^{-1}]	877	1000	~0.01	~0.1	~25	~1000	100	~0.001
I_{ON}/I_{OFF} Ratio [decades]	3.7	6	8	7	~5.5	2	3	6
Sub-threshold swing (S) [c] [mV dec^{-1}]	80	81	-	120	190	-	140	0.3 nF cm^{-2}
Hole Mobility [cm^2 V^{-1} s^{-1}]	43	51	-	680 (electron-linear)	400 (electron-linear)	105 (electron-linear)	70–80	1.6 (linear)
Minimum bending radius [mm]	5 (0.17% strain)	-	-	6.35 (0.13% strain)	-	8 (0.6% strain)	5	-

[a] n-MOS device [b] Estimated [c] Performance Indicator: how quickly a transistor can switch between ON and OFF state.

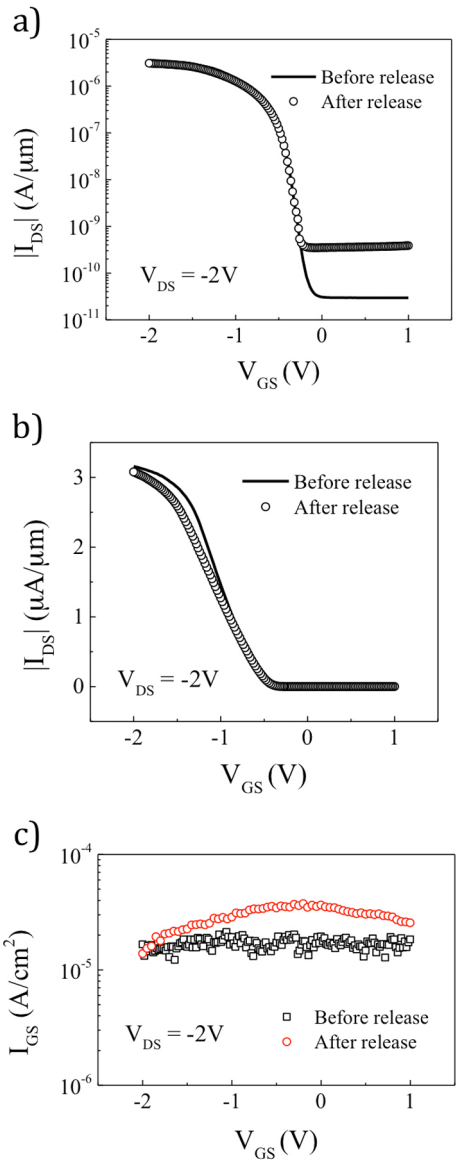

Figure 4 | Electrical performance comparison of a device before and after release. (L = 9 μm, W = 5 μm). (a) I_D–V_G transfer characteristics in logarithmic scale. (b) I_D–V_G transfer characteristics in linear scale. (c) Gate leakage density current.

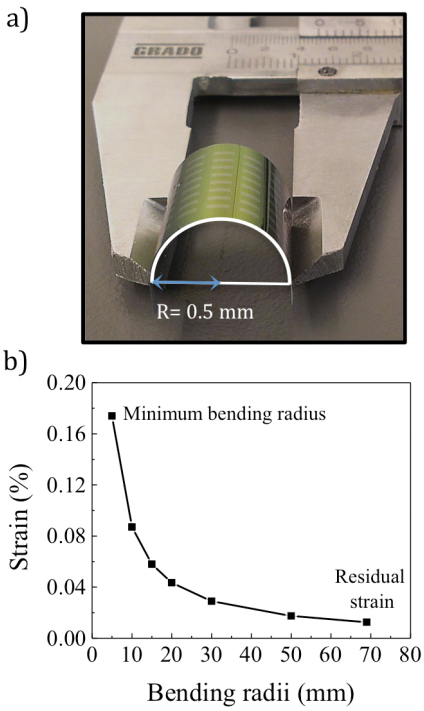

Figure 5 | (a) Silicon fabric bended at minimum bending radius of 5 mm. (b) Nominal strain dependence on bending radii.

(10, 15, 20, 30 and 50 mm, or their equivalent in nominal strain as in Fig. 5b). As illustration, the setup for the characterization of a transistor at a bending radius of 15 mm is shown Figure 6a. Figure 6b shows the behavior of the off-current and on-current in saturation region under different strain levels. At the maximum measured strain, I_{on} reduces less than 9% whereas I_{off} increases around 15%. As can be observed the increase in strain is related to a reduction in on state current, which was also observed on the sample after release due to the residual strain. Following the procedures described earlier, we have calculated the values for threshold voltage (V_{th}), sub-threshold swing (S) and effective mobility (μ_{eff}). Figure 6c shows a minor increase for both V_{th} and S of around 2%. On the other hand, variation in mobility versus gate voltage (equation (2)) for different strain conditions is shown in Figure 6d. There is a small reduction of mobility with higher strain (~8%), which is more evident at gate voltages closer to V_{th}. Overall, these results demonstrate the operation of the transistors under stressful conditions with only minimal changes in electrical performance. Additionally, the results concur with previous studies on stress/strain influence on electrical performance of MOSFET devices, where longitudinal tensile stress produces a reduction in drain saturation current and effective mobility, and no appreciable change in threshold voltage[31].

Optical characterization. An interesting consequence of having holes etched through the whole substrate is the apparent notion of semi-transparency in a solid opaque material such silicon (Fig. 7a). The reason why this happens is that light can pass through the densely packed holes allowing us to discern what is behind the sample. Optical transmittance in the visible range of the spectrum is shown in Figure 7b. The holes represent and empty area of about 25% of the whole sample, nevertheless only an average of 7% of light gets transmitted. Inset in Figure 7b helps to elucidate this behavior. Light gets diffracted and is dispersed into its components similar as with a compact disc. This behavior is characteristic of a diffraction grating in which the light is diffracted depending upon the spacing of the grating and the wavelength of the light[32]. This is also the reason why some wavelengths get transmitted more than others in Figure 7b.

Discussion

Many exciting applications have been demonstrated and pursued in the area of flexible electronics. In that realm, we show the process which uniquely distinguishes itself to offer the most pragmatic path for a truly high performance computer which is flexible and semi-transparent by using semiconductor industries' first choice: low-cost bulk mono-crystalline silicon (100) wafer, advanced high-k/metal gate stacks, uncompromising lithographic resolution, and conventional batch fabrication to extend the digital era to ultra-mobile digital age by converting modern silicon electronics into flexible and transparent one. The electrical superiority of inorganic semiconducting materials and the maturity of the semiconductor process technology make silicon the first choice to host high-performing transistors, and provide at the same time a mechanically robust support. We have chosen p-type transistors since they have been less studied and usually show lower current generation than

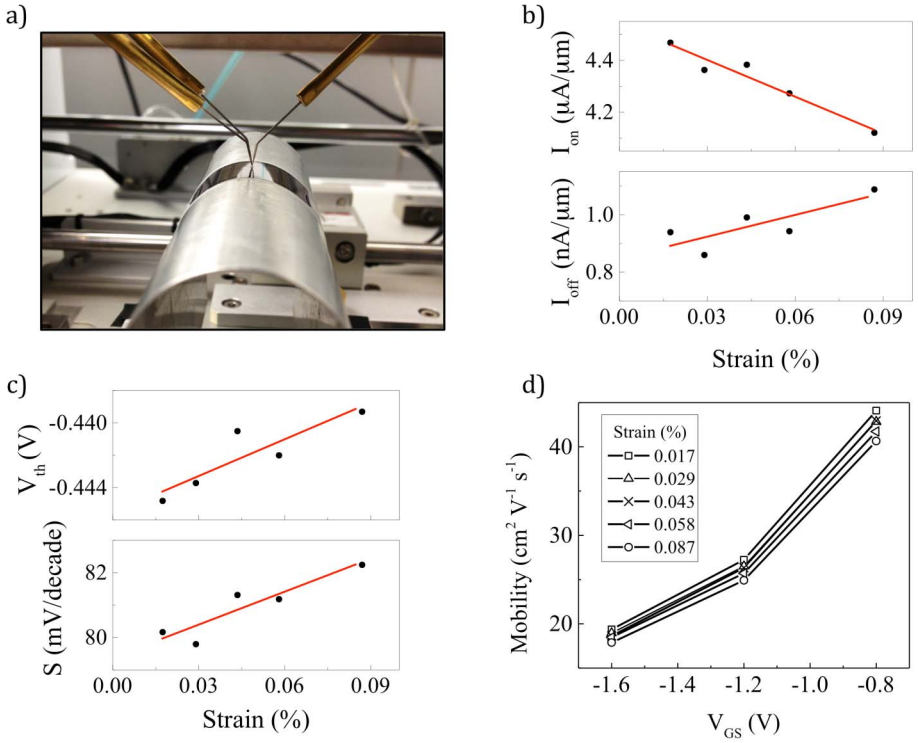

Figure 6 | Bendability dependence of electrical properties of the transistor. (a) Electrical measurement setup of a silicon fabric at 15 mm bending radius. (b) I_{on} and I_{off} behavior under different strain conditions. (c) V_{th} and S behavior under different strain conditions. (c) Effective mobility versus gate voltage curves for several strain conditions.

n-MOSFETs, demonstrating thus the ability of our processes and set of materials to perform well even with more challenging devices. In addition p-type MOSFETs are larger in size and by successfully demonstrating them we show that our process can integrate both the large as well as the smaller size devices. The fabricated transistors feature the most novel selection of materials, high-k/metal gate-stack, currently being used in semiconductor industry to overcome ultra-scaling issues related to unwanted leakage-induced excessive power dissipation, introduced due to short-channel and quantum effects. Electrical characterization of our devices (gate length of 8 μm and width of only 5 μm) shows a sub-threshold swing of 80 mV dec^{-1} and I_{on}/I_{off} ratio of near 10^4. The successfully released silicon *fabric* has an area of 3.75 cm^2 (2.5 cm × 1.5 cm), a thickness of ~15 μm and is capable of achieving bending radius as small as 5 mm (0.17% strain). Moreover, the fabric also displays semitransparency with an average transmittance of ~7% in the visible spectrum. These results demonstrate not only competitive electrical behavior but also outstanding bendability and modest degree of transparency, pointing out the fact that we rely only on inorganic material like silicon. Furthermore, our process allows reusing the same substrate to produce several thin substrates of functioning devices by chemical mechanical polishing of remaining wafers after the layers are peeled and released, indicating an economical advantage. We believe this opens up the possibility of producing high performance applications, in a cost effective and simple manner, for the expanding market of transparent, flexible electronics.

Methods

MOSFET fabrication. We started the fabrication with thermally oxidized (300 nm SiO_2) lightly doped (10–20 Ω.cm) 4″ n-type Si (100) wafer. The oxidation process takes place in a tube furnace at 1100°C by dry oxidation (3000 sccm O_2 for 15 minutes) then wet oxidation (200 sccm O_2 for 26 minutes), next dry oxidation (3000 sccm O_2 for 15 minutes) and finally an annealing step (5000 sccm N_2 for 20 minutes). Next, PR is coated and patterned (MicroChemicals©, 4 ml ECI 3027, 4 μm: 1750 rpm for 30 seconds, soft-bake: 100°C for 60 seconds) so trenches were made in the silicon dioxide layer using RIE (1500 W_{ICP}, 100 W_{RF}, 10 mTorr, 40 sccm C_4F_8, 5 sccm O_2). After the active area was prepared with RCA cleaning (SPM @ 120°C for 10 minutes, SC1 @ 75°C for 10 minutes, Diluted-HF @ RT for 30 seconds, SC2 @ 75°C for 10 minutes and Vapor HF @ 40°C for 30 seconds) (SPM = H_2SO_4/H_2O_2 – 4 : 1; SC1 = $NH_4OH/H_2O_2/H_2O$ – 1 : 1 : 20; SC2 = $HCl/H_2O_2/H_2O$ – 1 : 1 : 20), high-k/metal gate stack was deposited by ALD at 300°C (10 nm Al_2O_3: 100 cycles, Trimethyl Aluminium (TMA) dose = 15 ms, 80 mTorr, 3 seconds O_2 plasma {15 mTorr, 300 W}; and 20 nm TaN: 200 cycles, Tantalum (V) Trisdimethylamido t-butylimide (TTAN) dose = 5 seconds, 80 mTorr, 4 seconds H_2 plasma {15 mTorr, 400 W}). Next, PR was spin-coated (MicroChemicals©, 4 ml AZ 1512, 1.4 μm: 3000 rpm for 30 seconds, soft-bake: 100°C for 60 seconds) and patterned, followed by RIE (2000 W_{ICP}, 50 W_{RF}, 10 mTorr, 10 sccm SF_6, 90 sccm CHF_3) of the deposited films. Ion-implantation (I/I) was performed at a dose of 5×10^{13} cm^2 with BF_2 at 10 KeV. Next, PR was removed in acetone (5 minutes) and SPM (120°C for 5 minutes), followed by RTP at 950°C for 30 seconds in Ar environment (200 sccm) for dopant activation. A fast diluted-HF dip was done for 15 seconds before nickel deposition by sputtering (20 nm, 400 W, 5 mTorr, 25 sccm Ar), followed by RTP (450°C for 30 seconds in Ar: 200 sccm). Nickel excess is removed with SPM (120°C for 5 minutes). Next aluminum was sputtered (200 nm, 500 W, 5 mTorr, 25 sccm Ar), followed by PR spin-coating and patterning (MicroChemicals©, 4 ml AZ 1512, 1.4 μm: 3000 rpm for 30 seconds, soft-bake: 100°C for 60 seconds). The aluminum was then etched in RIE (Step 1: 80°C, 1500 W_{ICP}, 50 W_{RF}, 40 mTorr, 10 sccm Cl_2, 40 sccm BCl_3, 10 sccm Ar; Step 2: 80°C, 1500 W_{ICP}, 150 W_{RF}, 20 mTorr, 40 sccm Cl_2, 10 sccm BCl_3; Step 3: 80°C, 1500 W_{ICP}, 50 W_{RF}, 40 mTorr, 10 sccm Cl_2, 30 sccm BCl_3, 20 sccm Ar; Step 4: 80°C, 150 W_{RF}, 900 mTorr, 100 sccm O_2). PR was removed in acetone (5 minutes in sonicator).

Release fabrication. Aluminum oxide was deposited by ALD (40 nm Al_2O_3: TMA for 15 ms, H_2O_{vapor} for 15 ms, 400 cycles at 250°C), as protection leyer. Then, a final PR layer is coated (MicroChemicals©, 4 ml AZ 1512, 2 μm: 1750 rpm for 30 seconds, soft-bake: 100°C for 60 seconds) and RIE of aluminum oxide (1000 W_{ICP}, 100 W_{RF}, 10 mTorr, 5 sccm Ar, 20 sccm CHF_3) and silicon dioxide (1500 W_{ICP}, 100 W_{RF}, 10 mTorr, 40 sccm C_4F_8, 5 sccm O_2) is done. BOSCH process is performed (120 cycles at −20°C; Etch step: 7 seconds, 1300 W_{ICP}, 30 W_{RF}, 35 mTorr, 5 sccm C_4F_8, 120 sccm SF_6; deposition step: 5 seconds, 1300 W_{ICP}, 5 W_{RF}, 35 mTorr, 100 sccm C_4F_8, 5 sccm SF_6) to form deep trenches (30 μm) into the substrate. Next, a second layer of Al_2O_3 is deposited by ALD (40 nm Al_2O_3: TMA for 15 ms, H_2O_{vapor} for 15 ms, 400 cycles at 250°C) to protect the sidewalls of the trenches. In order to permit access for XeF_2 etchant to the bottom of the trenches, directional RIE process is performed (1000 W_{ICP}, 100 W_{RF}, 3 mTorr, 5 sccm Ar, 20 sccm CHF_3), to remove the Al_2O_3 layer from the bottom of the deep trenches leaving the sidewalls protected. XeF_2 etching (4.5 Torr, 60 seconds/cycle, 60 cycles) is used to release a thin fabric by

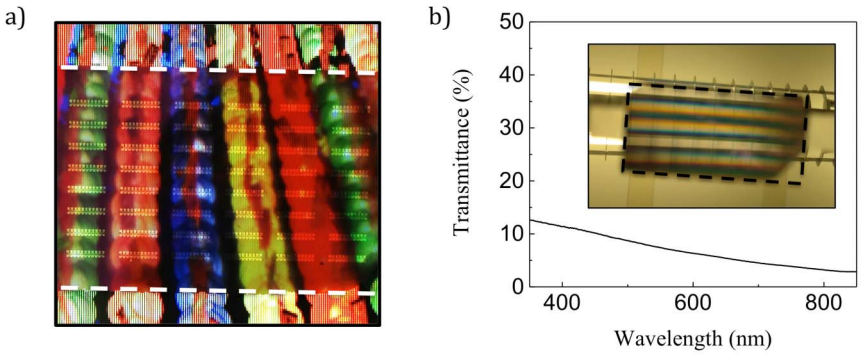

Figure 7 | Optical characterization. (a) Silicon fabric with devices (delimited with dashed lines) on top of LED screen showing semi-transparency. (b) Light transmittance versus wavelength in the visible range (Inset-Silicon fabric with devices (delimited with dashed lines) showing diffraction and separation of light into its components as with a diffraction grating).

isotropically etching silicon from the accessible portion of the bulk substrate in the bottom of the trenches. Finally, forming gas anneal (FGA) is performed (400°C for 5 minutes in Ar: 200 sccm).

Electrical, mechanical and optical measurements. I–V characteristics were measured with a semiconductor parameter analyzer (Keithley 4200-SCS) attached to a probe station (Cascade). For electrical performance dependence on bending radii study we designed plates with specific bending radius where we attached the samples and then performed electrical characterization. Optical transmittance was measured with a spectrophotometer (Thermo scientific, 300 Evolution UV-Vis).

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Author contributions

M.H. conceptualized and directed the project. J.P.R. carried out the experiment. G.A.T.S. developed the recylcing process and assisted in the experiment. All analyzed the data and co-authored.

Additional information

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